REMARKS

This Amendment responds to the final Office Action mailed on November 14, 2008 and is being enclosed with a Request for Continued Examination submitted concurrently herewith. This Amendment represents a fully responsive submission, as required under 37 CFR § 1.114. Claim 1, 3, 5-13, 19, and 34-42 are pending. Claims 9-13 and 36-42 are withdrawn. Claims 1, 3, 5-13, 19, and 34-42 have been amended. Claims 15-18, 20, 43, 44, 46-48, 52, and 53 have been cancelled. In view of the following remarks, as well as the preceding amendments, Applicants respectfully submit that this application is in complete condition for allowance and request reconsideration of the application in this regard.

Rejections Under 35 U.S.C. § 103

Claims 1, 3, 5-8, 15-19, 34, 35, 43, 44, 46-48, 52, and 53 over Choi and Occhipinti

Claims 1, 3, 5-8, 15-19, 34, 35, 43, 44, 46-48, 52, and 53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Choi et al. (U.S. Patent No. 6,566,704), hereinafter *Choi*, in view of U.S. Publication No. 2004/0027889 to Occhipinti et al. (hereinafter *Occhipinti*). Claim 1 is the sole independent claim. Applicants respectfully traverse the rejection for the reasons set forth below.

Choi fails to disclose "a dielectric-filled space between said vertical sidewall of said first gate electrode and said vertical sidewall of said second gate electrode, said at least one first semiconducting carbon nanotube disposed within said dielectric-filled space", as set forth in as-amended claim 1. Instead, *Choi* discloses a structure in FIGS. 1 and 3F in which the nanotube (100) of each transistor extends through a central hole or opening in a gate electrode (20). Because the nanotube (100) is surrounded by the conductive material of the gate electrode (20), the nanotube (100) is not located in a dielectric-filled space between the respective vertical

sidewalls of the gate electrodes of different transistors. Figures 4A and 4B of *Choi* teach that a device construction the gate electrode (20) is disposed above the nanotubes (100). In this device construction, the nanotube (100) is not located in a dielectric-filled space between the respective vertical sidewalls of the gate electrodes of different transistors. *Occhipinti* fails to remedy this deficiency of *Choi*.

The Examiner has failed to establish a *prima facie* case of obviousness because this deficiency of *Occhipinti* and *Choi* in comparison with claim 1 evidences a failure to resolve the *Graham* factual inquiries. For this reason, Applicants request that the Examiner withdraw the rejection.

As stated in the Background section of Applicants' specification, "[i]n certain FET designs, the catalyst material may be located at the base of a high-aspect-ratio opening, which further restricts reactant flow." *Choi* states that "[a]s shown in FIG. 3C, a carbon nanotube 100 is vertically grown on the source 40 in the hole 10' by CVD, electrophoresis or mechanical compression". *See* col. 4, lines 21-25. *Choi* also disclosed that "[f]irst, carbon nanotubes 100 are grown on a nonconductor substrate 10 having nano-sized holes (not shown) and arranged by vertical growth and selective deposition." *See* col. 4, lines 40-42. These disclosures are typical of convention approaches discussed in the Background section of Applicants' specification. *Choi* fails to disclose that the nanotubes (100) are grown in a space, which is eventually dielectric filled, between the respective vertical sidewalls of the gate electrodes of different transistors.

Because claims 3, 5-8, 19, 34, and 35 depend from independent claim 1, Applicants submit that these claims are also patentable for at least the same reasons discussed above. Furthermore, each of these dependent claims recites a unique combination of elements not disclosed or suggested by the combination of *Choi* and *Occhipinti*.

Claims 5, 6, 34, and 46 over Choi, Occhipinti, and Farnworth

Claims 5, 6, 34, and 46 stand rejected under 35 U.S.C. § 103(a) as being unpatentable *Choi* and *Occhipinti* further in view of Farnworth et al. (U.S. Patent No. 6,515,325), hereinafter *Farnworth*. Claim 46 is cancelled. Because claims 5, 6, and 34 depend from independent claim 1, Applicants submit that these dependent claims are patentable for at least the same reasons. Furthermore, these dependent claims recite unique combinations of elements not taught, disclosed or suggested by the combination of *Choi*, *Occhipinti*, and *Farnworth*.

Conclusion

Applicants have made a bona fide effort to respond to each and every requirement set forth in the Office Action. In view of the foregoing remarks and amendments, this application is submitted to be in complete condition for allowance. Accordingly, a timely notice of allowance to this effect is earnestly solicited. In the event that any issues remain outstanding, the Examiner is invited to contact the undersigned to expedite issuance of this application.

Applicants do not believe any fees are due in connection with filing this communication other than the fee for filing a Request for Continued Examination. If, however, any fees are necessary as a result of this communication, the Commissioner is hereby authorized to charge any under-payment or fees associated with this communication or credit any over-payment to Deposit Account No. 23-3000.

Respectfully submitted,

January 19, 2009
Date

/William R. Allen/
William R. Allen, Ph.D.
Reg. No. 48,389

WOOD, HERRON & EVANS, L.L.P.
2700 Carew Tower
441 Vine Street
Cincinnati, Ohio 45202
Telephone: (513) 241-2324
Facsimile: (513) 241-6234